

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

5 peripheral electrodes formed on a periphery of

 a semiconductor chip;

 internal electrodes formed inside the
 peripheral electrodes on the semiconductor chip; and
 circuits formed in the semiconductor chip,

10 wherein the peripheral electrodes are connected
 to the circuits by an internal line, and the internal
 electrodes are connected to the circuits and the
 peripheral electrodes by the internal line.

15 2. A semiconductor device according to Claim
 1, wherein the internal electrodes are smaller than
 the peripheral electrodes.

20 3. A semiconductor device according to Claim
 1, wherein the internal electrodes comprise at least
 one selected from the group consisting of a power
 supply terminal, a ground terminal, and a clock
 terminal.

25 4. A semiconductor device according to Claim
 1, wherein the peripheral electrodes not connected
 to the internal electrodes are used as terminals for
 high-frequency signals.

5. A semiconductor device comprising:
peripheral electrodes formed on a periphery of
a semiconductor chip;

5 internal electrodes formed inside the
peripheral electrodes on the semiconductor chip; and
circuits formed in the semiconductor chip,
wherein the peripheral electrodes are connected
to the circuits by an internal line, the internal
10 electrodes are connected to the circuits and the
peripheral electrodes by the internal line, and the
internal electrodes are also connected to rewired
lines, the rewired lines formed above the internal
electrodes with an insulating layer therebetween,
15 and at ends of the rewired lines formed area array
electrodes.

6. A semiconductor device comprising:
peripheral electrodes formed on a periphery of
20 a semiconductor chip;
internal electrodes formed inside the
peripheral electrodes on the semiconductor chip;
area array electrodes connected to selected one
of the peripheral electrodes and the internal
25 electrodes and formed on the semiconductor chip; and
circuits formed in the semiconductor chip,

wherein the peripheral electrodes are connected to the circuits by an internal line, the internal electrodes are connected to the circuits and the peripheral electrodes by the internal line, and the area array electrodes comprise first area array electrodes connected to the internal electrodes by rewired lines and second area array electrodes connected to the peripheral electrodes by rewired lines.

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7. A semiconductor device according to Claim 6, wherein the first area array electrodes comprise at least one selected from the group consisting of a power supply terminal, a ground terminal, and a clock terminal.

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8. A semiconductor device according to Claim 6, wherein the second area array electrodes are used as terminals for high-frequency signals.

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